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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,079	07/31/2003	Gerard Chauvel	TI-35425 (1962-05404)	2206

23494 7590 08/26/2005

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EXAMINER	
NGUYEN, HIEP T	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 08/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/632,079	CHAUVEL ET AL.	
	Examiner	Art Unit	
	Hiep T. Nguyen	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/31/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are presented for examination.
2. Applicant is required to provide the application numbers [when the become available] for the copending applications cited on pages 1-3 of the specification.

Priority

3. Receipt is acknowledged of papers filed under 35 U.S.C. 119 (a)-(d) based on an application filed in European on July 30, 2003. Applicant has not complied with the requirements of 37 CFR 1.63(c), since the oath, declaration or application data sheet does not acknowledge the filing of any foreign application. A new oath, declaration or application data sheet is required in the body of which the present application should be identified by application number and filing date.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

    a. A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayes et al., U.S. Patent No. 5,107,457 [hereafter, Hayes] in view of well-known features of which Official notice is hereby taken.

    a. <u>As per claim 1:</u>

        i. Hayes teaches a system [figure 1], comprising:

            1. A main stack (16);

            2. Micro-stack (10) coupled to the main stack;

3. A stack pointer (12);
4. Wherein the micro-stack resides in the core of a processor and the main stack resides outside of the core of the processor [col. 3, lines 20-26];
5. Wherein the stack pointer indicates the top of the main stack [see figure 1].

ii. Hayes, however, does not teach a data flag coupled to the micro-stack to indicate valid data in the micro-stack.

iii. Valid status data associated with internal cache has been commonly practice in the pertinent art. Obviously the use of valid indicating information is to identify which data entry in the cache is valid so that to determine whether a requested data should be provided from the cache or from the external memory. Furthermore, with the use of the valid indicating information would further instruct the system to only write back the valid data to the external memory when the cache is flushed.

iv. Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further employ valid indicating information for each of the cache entry of the Hayes internal stack cache. The ability to determine whether to provide the requested data from the cache or from external memory and to write back only valid data when the cache is flushed provide sufficient suggestion and motivation to one having ordinary skill in the art at the time the invention was made to do such valid indicating information employment in the Hayes system.

b. As per claims 2-3: Hayes also teaches a computing engine [i.e., processor core] coupled to the micro-stack.

c. As per claim 4: writing back date from an internal cache to an external memory responsive to a cache flush has also been commonly practiced in the pertinent art. Accordingly, it would have been obvious to one having ordinary skill in the art to further

employ logic into the Hayes cache to write back data from the internal stack to the external memory responsive to an internal cache flush.

d. As per claim5: Hayes further teaches that data is written to the micro-stack during an overflow condition [se co. 3, lines 44-58].

e. As per claims 6-7: similarly to claim 4, data flag indicating coherence [e.g., modified indicating bit] indicating coherency between the main memory and an internal cache has also been commonly practiced in the pertinent art. Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further employ data flag for indicating the coherence between the Hayes internal stack (10) and external memory stack (16).

f. As per claims 8-9: the further claimed limitations are directly taught by Hayes through overflow and underflow conditions.

g. As per claim 10: there is no specific size is being claimed for the micro stack. Utilize a small cache for faster look up and/or lager size cache for a better cache hit has also been commonly known in the pertinent art. Accordingly, it would have obvious to one having ordinary skill in the pertinent art to select a cache size that is optimized for increased performance depending on the application being used.

h. As per claims 11-20: the claimed method basically encompasses the steps that are carried out by the corresponding elements in the claims 1-10. Accordingly, claims 11-20 are also rejected for the same reasons as set forth for that in claims 1-10.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. O'Conner e al., 5,970,242, teaches an internal stack cache with a valid bit indicting if a stack entry in the stack cache is valid.

b. Vishin, 6,219,757, teaches an internal stack cache having a valid bit for each cache entry.

c. Tran, 6,604,190, teaches a stack cache that writes back modified data to external memory.

d. Mackenthun et al., 6,868,482, teaches a cache system that flushes back only valid cache lines to the external memory.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep T. Nguyen whose telephone number is (571) 272-4197. The examiner can normally be reached on Monday-Friday from 9:30 am to 6:00 pm.

8. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep T Nguyen
Primary Examiner
Art Unit 2187

HTN